Amendments to the Claims:

Please cancel claims 81-89 and amend claims 4, 5, 6, 12, 15, 16, 18-28, 30-32, 34-44, 46-48, 50-60, 62-64, 66-76, 78-80 as follows:

Listing of Claims:

1. (Original) An integrated circuit package assembly for electrically isolating modules, comprising:

a substrate having a first side and an opposing second side;

a first module attached to the first side of the substrate;

a second module attached to the first side of the substrate;

a first conductive surface proximate to the second side of the substrate, the first conductive surface conductively coupled to the first module; and

a second conductive surface spaced apart from the first conductive surface to form a capacitor with the first conductive surface, the second conductive surface being coupled to the second module.

2. (Original) The package assembly of claim 1, further comprising a dielectric interposed between the first and second conductive surfaces.

3. (Original) The package assembly of claim 1, further comprising an encapsulation substantially surrounding the package assembly.

4. (Currently Amended) The package assembly of claim 3 wherein the ~~package assembly is encased in a polymer~~ encapsulation further comprises a polymer that encases the package assembly.

5. (Currently Amended) The package assembly of claim 3 wherein the ~~package assembly is encased in ceramic~~ encapsulation further comprises a ceramic that encases the package assembly.

6. (Currently Amended) The package assembly of claim 3 wherein the ~~package assembly is encased in a glass~~ encapsulation further comprises a glass that encases the package assembly.

7. (Original) The package assembly of claim 1 wherein the first module is an integrated circuit.

8. (Original) The package assembly of claim 7 wherein the integrated circuit is a physical layer chip.

9. (Original) The package assembly of claim 1 wherein the second module is an integrated circuit.

10. (Original) The package assembly of claim 9 wherein the integrated circuit is a link layer chip.

11. (Original) The package assembly of claim 1, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

12. (Currently Amended) The package assembly of claim [[10]] 11 wherein the resistor has a resistance of approximately one megohm.

13. (Original) The package assembly of claim 11 wherein the resistor is a resistant film.

14. (Original) The package assembly of claim 1, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

15. (Currently Amended) The package assembly of claim [[13]] 14 wherein the first ground plane comprises a ground wire of a cable bus.

16. (Currently Amended) The package assembly of claim [[13]] 14 wherein the second ground plane comprises a chassis of a computer.

17. (Original) An integrated circuit package assembly for electrically isolating integrated circuits within a module, comprising:

a substrate having a first side and an opposing second side;

a module attached to the first side of the substrate, the module having a first and second integrated circuit;

a first conductive surface proximate to the second side of the substrate, the first conductive surface conductively coupled to the first integrated circuit; and

a second conductive surface spaced apart from the first conductive surface to form a capacitor with the first conductive surface, the second conductive surface being conductively coupled to the second integrated circuit.

18. (Currently Amended) The package assembly of claim [[16]] 17, further comprising a dielectric interposed between the first and second conductive surfaces.

19. (Currently Amended) The package assembly of claim [[16]] 17, further comprising an encapsulation substantially surrounding the package assembly.

20. (Currently Amended) The package assembly of claim [[18]] 19 wherein the ~~package assembly is encased in a polymer~~ encapsulation further comprises a polymer that encases the package assembly.

21. (Currently Amended) The package assembly of claim [[18]] 19 wherein the ~~package assembly is encased in ceramic~~ encapsulation further comprises a ceramic that encases the package assembly.

22. (Currently Amended) The package assembly of claim [[18]] 19 wherein the ~~package assembly is encased in a glass~~ encapsulation further comprises a glass that encases the package assembly.

23. (Currently Amended) The package assembly of claim [[16]] 17 wherein the first module is an integrated circuit.

24. (Currently Amended) The package assembly of claim [[22]] 23 wherein the integrated circuit is a physical layer chip.

25. (Currently Amended) The package assembly of claim [[16]] 17 wherein the second module is an integrated circuit.

26. (Currently Amended) The package assembly of claim [[24]] 25 wherein the integrated circuit is a link layer chip.

27. (Currently Amended) The package assembly of claim [[16]] 17, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

28. (Currently Amended) The package assembly of claim [[26]] 27 wherein the resistor has a resistance of approximately one megohm.

29. (Original) The package assembly of claim 27 wherein the resistor is a resistant film.

30. (Currently Amended) The package assembly of claim [[16]] 17, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

31. (Currently Amended) The package assembly of claim [[28]] 30 wherein the first ground plane comprises a ground wire of a cable bus.

32. (Currently Amended) The package assembly of claim [[28]] 30 wherein the second ground plane comprises a chassis of a computer.

33. (Original) An integrated circuit package assembly for electrically isolating modules, comprising:

a first substrate with a first and opposing second side having a first module attached to the first side;

a first conductive surface proximate to the second side of the first substrate, the first conductive surface being conductively coupled to the first module;

a second substrate with a first and opposing second side having a second module attached to the first side; and

a second conductive surface proximate to the opposing side of the second substrate, the second conductive surface being conductively coupled to the second module and spaced apart from the first conductive surface to form a capacitor with the first conductive surface.

34. (Currently Amended) The package assembly of claim [[31]] 33, further comprising a dielectric interposed between the first and second conductive surfaces.

35. (Currently Amended) The package assembly of claim [[31]] 33, further comprising an encapsulation substantially surrounding the package assembly.

36. (Currently Amended) The package assembly of claim [[33]] 35 wherein the ~~package assembly is encased in a polymer~~ encapsulation further comprises a polymer that encases the package assembly.

37. (Currently Amended) The package assembly of claim [[33]] 35 wherein the ~~package assembly is encased in ceramic~~ encapsulation further comprises a ceramic that encases the package assembly.

38. (Currently Amended) The package assembly of claim [[33]] 35 wherein the ~~package assembly is encased in a glass~~ encapsulation further comprises a glass that encases the package assembly.

39. (Currently Amended) The package assembly of claim [[31]] 33 wherein the first module is an integrated circuit.

40. (Currently Amended) The package assembly of claim [[37]] 39 wherein the integrated circuit is a physical layer chip.

41. (Currently Amended) The package assembly of claim [[31]] 33 wherein the second module is an integrated circuit.

42. (Currently Amended) The package assembly of claim [[39]] 41 wherein the integrated circuit is a link layer chip.

43. (Currently Amended) The package assembly of claim [[31]] 33, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

44. (Currently Amended) The package assembly of claim [[41]] 43 wherein the resistor has a resistance of approximately one megohm.

45. (Original) The package assembly of claim 43 wherein the resistor is a resistant film.

46. (Currently Amended) The package assembly of claim [[31]] 33, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

47. (Currently Amended) The package assembly of claim [[43]] 46 wherein the first ground plane comprises a ground wire of a cable bus.

48. (Currently Amended) The package assembly of claim [[43]] 46 wherein the second ground plane comprises a chassis of a computer.

49. (Original) An integrated circuit package assembly for electrically isolating integrated circuits within a module, comprising:

a substrate;

a first module having a first and opposing second side attached to the substrate on the first side;

a second module having a first and opposing second side attached to the substrate on the first side;

a non-conductive layer having a first and opposing second side, the first side proximate to the opposing second sides of the first and second modules;

a first conductive surface proximate to the second side of the first non-conductive layer, the first conductive surface conductively coupled to the first module; and

a second conductive surface spaced apart from the first conductive surface to form a capacitor with the first conductive surface, the second conductive surface being conductively coupled to the second module.

50. (Currently Amended) The package assembly of claim [[46]] 49, further comprising a dielectric interposed between the first and second conductive surfaces.

51. (Currently Amended) The package assembly of claim [[46]] 49, further comprising an encapsulation substantially surrounding the package assembly.

52. (Currently Amended) The package assembly of claim [[48]] 51 wherein the ~~package assembly is encased in a polymer~~ encapsulation further comprises a polymer that encases the package assembly.

53. (Currently Amended) The package assembly of claim [[48]] 51 wherein the ~~package assembly is encased in ceramic~~ encapsulation further comprises a ceramic that encases the package assembly.

54. (Currently Amended) The package assembly of claim [[48]] 51 wherein the ~~package assembly is encased in a glass~~ encapsulation further comprises a glass that encases the package assembly.

55. (Currently Amended) The package assembly of claim [[46]] 49 wherein the first module is an integrated circuit.

56. (Currently Amended) The package assembly of claim [[52]] 55 wherein the integrated circuit is a physical layer chip.

57. (Currently Amended) The package assembly of claim [[46]] 49 wherein the second module is an integrated circuit.

58. (Currently Amended) The package assembly of claim [[54]] 57 wherein the integrated circuit is a link layer chip.

59. (Currently Amended) The package assembly of claim [[46]] 49, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

60. (Currently Amended) The package assembly of claim [[56]] 59 wherein the resistor has a resistance of approximately one megohm.

61. (Original) The package assembly of claim 59 wherein the resistor is a resistant film.

62. (Currently Amended) The package assembly of claim [[46]] 49, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

63. (Currently Amended) The package assembly of claim [[58]] 62 wherein the first ground plane comprises a ground wire of a cable bus.

64. (Currently Amended) The package assembly of claim [[58]] 62 wherein the second ground plane comprises a chassis of a computer.

65. (Original) An integrated circuit package assembly for electrically isolating modules, comprising:

a substrate having a first side and an opposing second side;

a first module having a first and opposing second side attached to the first side of the substrate on the first side of the first module;

a second module attached to the second side of the first module;

a first conductive surface proximate to the second side of the substrate, the first conductive surface conductively coupled to the first module; and

a second conductive surface spaced apart from the first conductive surface to form a capacitor with the first conductive surface, the second conductive surface being coupled to the second module.

66. (Currently Amended) The package assembly of claim [[61]] 65, further comprising a dielectric interposed between the first and second conductive surfaces.

67. (Currently Amended) The package assembly of claim [[61]] 65, further comprising an encapsulation substantially surrounding the package assembly.

68. (Currently Amended) The package assembly of claim [[63]] 67 wherein the ~~package assembly is encased in a polymer~~ encapsulation further comprises a polymer that encases the package assembly.

69. (Currently Amended) The package assembly of claim [[63]] 67 wherein the ~~package assembly is encased in ceramic~~ encapsulation further comprises a ceramic that encases the package assembly.

70. (Currently Amended) The package assembly of claim [[63]] 67 wherein the ~~package assembly is encased in a glass~~ encapsulation further comprises a glass that encases the package assembly.

71. (Currently Amended) The package assembly of claim [[61]] 65 wherein the first module is an integrated circuit.

72. (Currently Amended) The package assembly of claim [[67]] 71 wherein the integrated circuit is a physical layer chip.

73. (Currently Amended) The package assembly of claim [[61]] 65 wherein the second module is an integrated circuit.

74. (Currently Amended) The package assembly of claim [[69]] 73 wherein the integrated circuit is a link layer chip.

75. (Currently Amended) The package assembly of claim [[61]] 65, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

76. (Currently Amended) The package assembly of claim [[71]] 75 wherein the resistor has a resistance of approximately one megohm.

77. (Original) The package assembly of claim 75 wherein the resistor is a resistant film.

78. (Currently Amended) The package assembly of claim [[61]] 65, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

79. (Currently Amended) The package assembly of claim [[73]] 78 wherein the first ground plane comprises a ground wire of a cable bus.

80. (Currently Amended) The package assembly of claim [[73]] 78 wherein the second ground plane comprises a chassis of a computer.

81-89. (Cancelled)